

REMARKS/ARGUMENTS

Claim 1 recites converting a configuration access corresponding to a memory address or I/O address to a configuration cycle for configuration of an integrated device of a first processor, and routing the configuration cycle directly from the decoder to the first processor based at least in part on routing information. The BIOS Guide nowhere teaches or suggests this subject matter. Specifically, there is no teaching of a configuration access that corresponds to a memory address or an IO address. Still further, the Guide fails to teach converting such access to a configuration cycle. The Guide instead simply teaches the conventional method of translating configuration cycles. Still further, the Guide fails to teach or suggest routing this converted configuration cycle directly from a decoder of a second processor to the first processor. As such, claim 1 and the claims depending therefrom are patentable over the cited art.

Regarding claim 6, the Guide fails to teach or suggest the recited decoding of a configuration access to a configuration cycle, as described above. Still further, there is no teaching in the Guide that such decoding includes retrieving a node identifier and port number using a configuration address associated with the configuration access. Still further, the Guide fails to teach the direct routing from a second processor to an integrated device in a first processor. Accordingly, claim 6 and its dependent claims are patentable over the cited art.

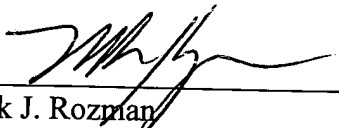
For at least similar reasons, independent claims 12, 15 and 18 are similarly patentable.

In view of these remarks, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504.

Respectfully submitted,

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